AU OPTRONICS CORPORATION

Product Specification

17.0” WXGA+ Color TFT-LCD Module

Model Name: B170PW03 V1

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Product Specification

17.0” WXGA+ Color TFT-LCD Module
Model Name: B170PW03
V.1

( ) Preliminary Specifications
(V) Final Specifications

Note: This Specification is subject to change without notice.

Contents

Record of Revision

Version and Date	Page	Old description	NPW Description	Remark
V1 2005/5/23	All	First Edition for Customer		
V2 2005/10/05	6	Weight: 700g max	Weight 690g max	
V3 2005/10/21	6	382.2(W) x 244.5(H) x 6.6(D) max	382.2(W) x 244.5(H) x 6.6(D) typ	
V4 2005/12/02	6	8.5 W max	7.5 W typ. (without inverter)	
	7	Constract Ratio min: 350	Constract Ration min: 300	
	26	Old PCB Cover Film	Add “Don’t Touch” mark to PCB Cover Film	
	28	Shipping Label Old Format	Add RoHS Mark	
V5 2006/6/22	7	White(X,Y) = (0.320, 0.330)	White(X,Y) = (0.313, 0.329)	
V6 2007/07/27	15	CCFL Voltage (Reference) (VCCFL)Min:775,TYP:815,MAX:940	CCFL Voltage (Reference) (VCCFL)Min:745,TYP:785,MAX:905	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

2. General Description

B170PW03 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA+ (1440(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B170PW03 V1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

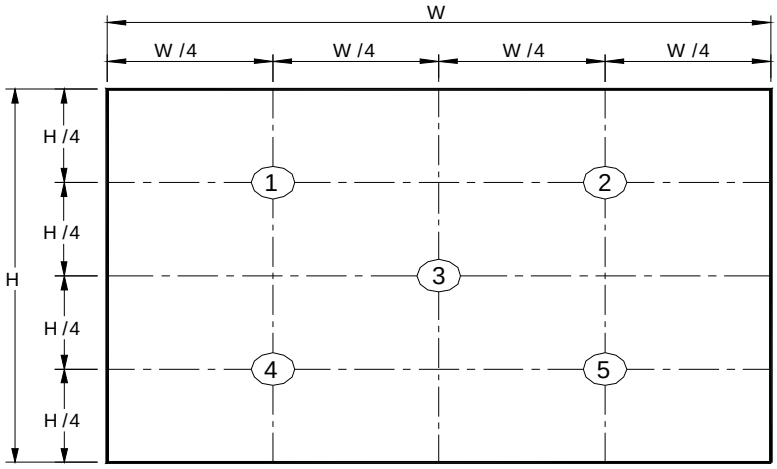
Items	Unit	Specifications
Screen Diagonal	[mm]	17.0”
Active Area	[mm]	367.20(H) x 229.50(V)
Pixels H x V		1440x3(RGB) x 900
Pixel Pitch	[mm]	0..255(per one triad) x 0.255
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (ICCFL=6.5mA)	[cd/m^2]	200 typ. (5 points average) 170 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ.
Response time	[msec]	16 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption	[Watt]	7.5W typ. (without inverter)
Weight	[Grams]	690 g max.
Physical Size	[mm]	382.2(W) x 244.5(H) x 6.6(D) typ..
Electrical Interface		2 channel LVDS
Surface Treatment		Glare
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Non-Operating)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

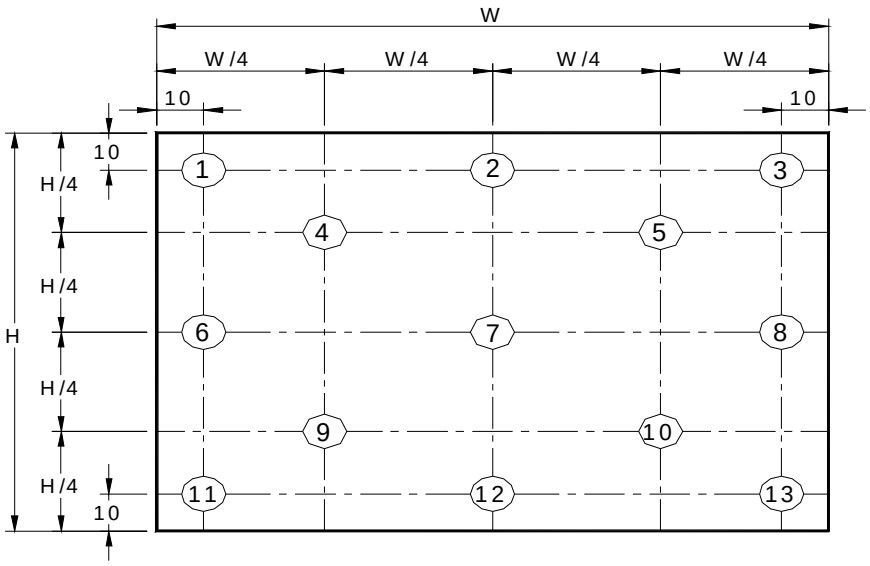
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Luminance ICCFL 6.5mA	[cd/m2]	5 points average	170	200	-	1,2,3
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	60 60	70 70	- -	2,7
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	50 50	60 60	- -	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			2.0	
CR: Contrast Ratio			300	400	-	6
Cross talk	%				4	4
Response Time	[msec]	Rising	-	12	17	5
	[msec]	Falling	-	4	8	
	[msec]	Raising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.550	0.580	0.610	2,7
		Red y	0.310	0.340	0.370	
		Green x	0.280	0.310	0.340	
		Green y	0.520	0.550	0.580	
		Blue x	0.120	0.150	0.180	
		Blue y	0.090	0.120	0.150	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 367.20(H) x 229.50(V)mm)



Note 2: 13 points position



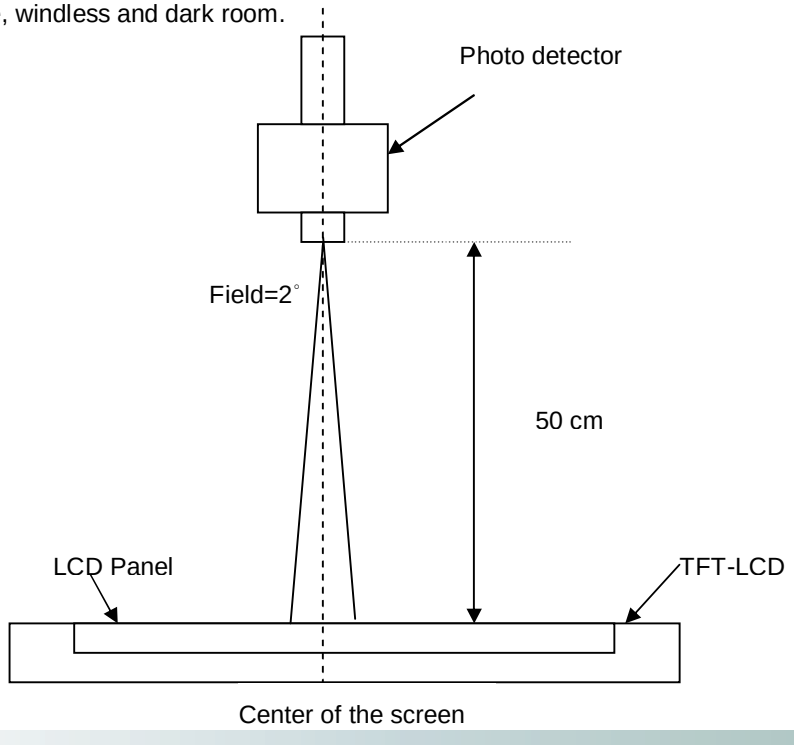
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



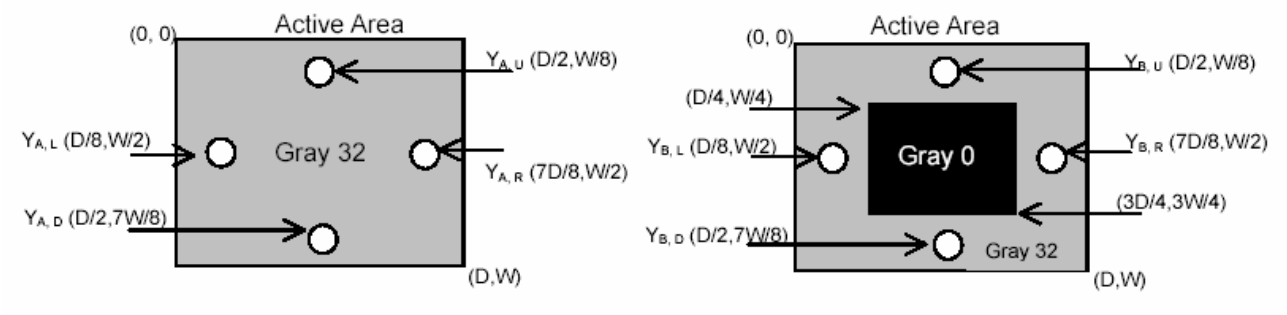
Note 5： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

Where

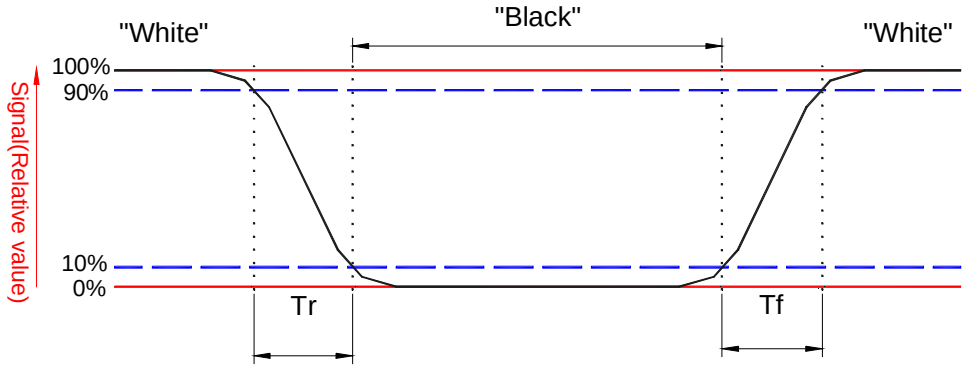
Y_A = Luminance of measured location without gray level 0 pattern (cd/m 2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m 2)



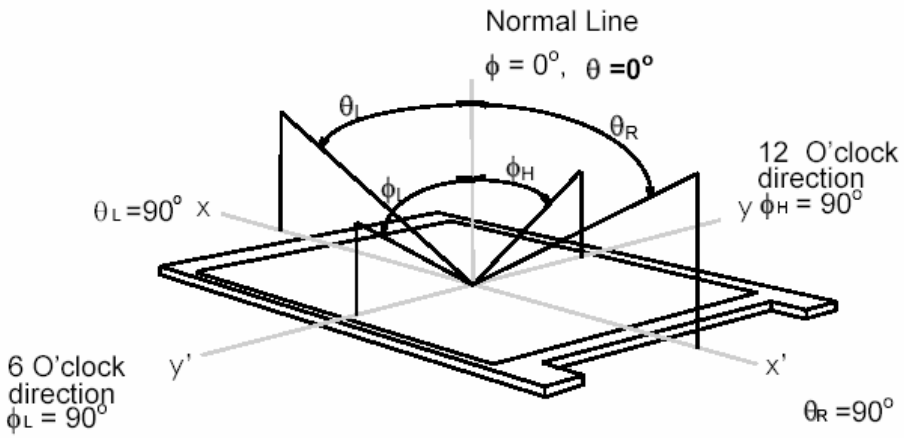
Note 6: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



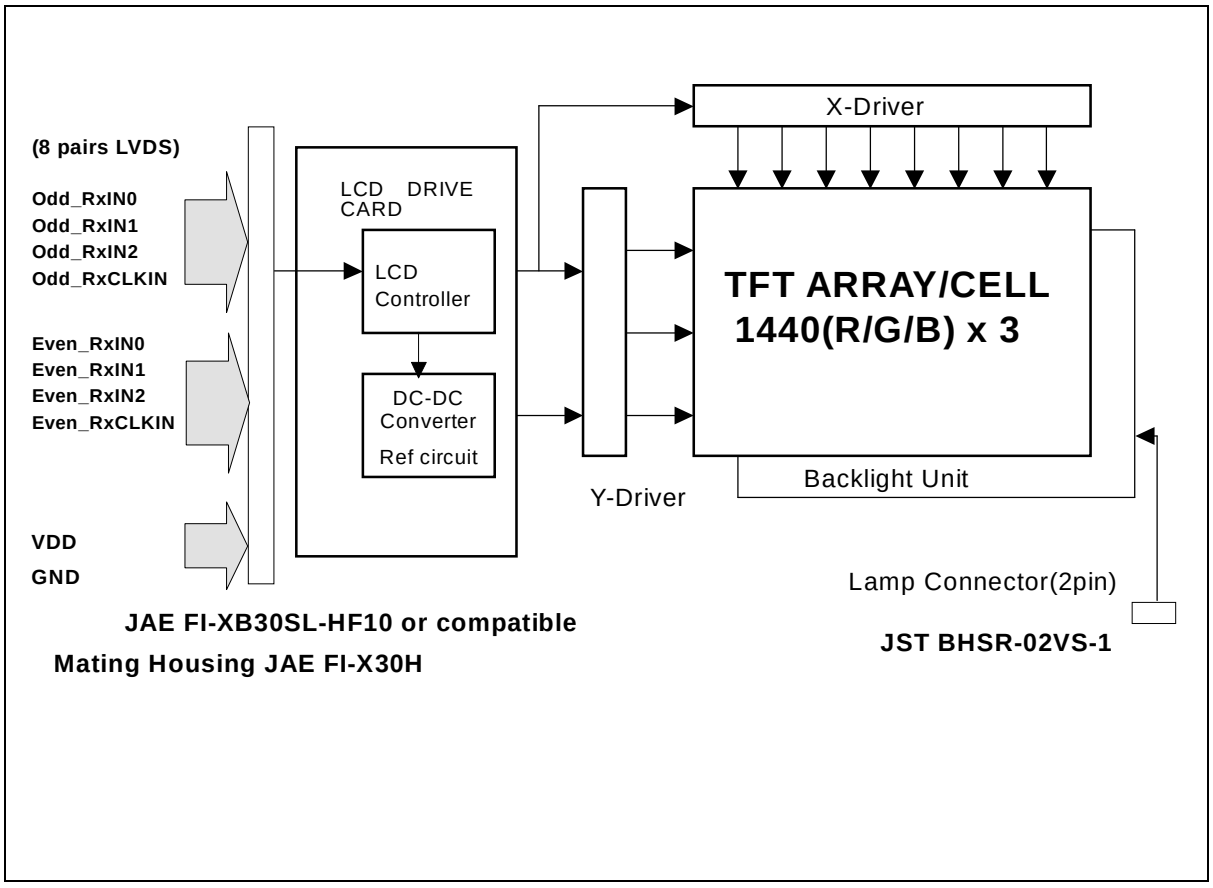
Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 17.0 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings ofBacklight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

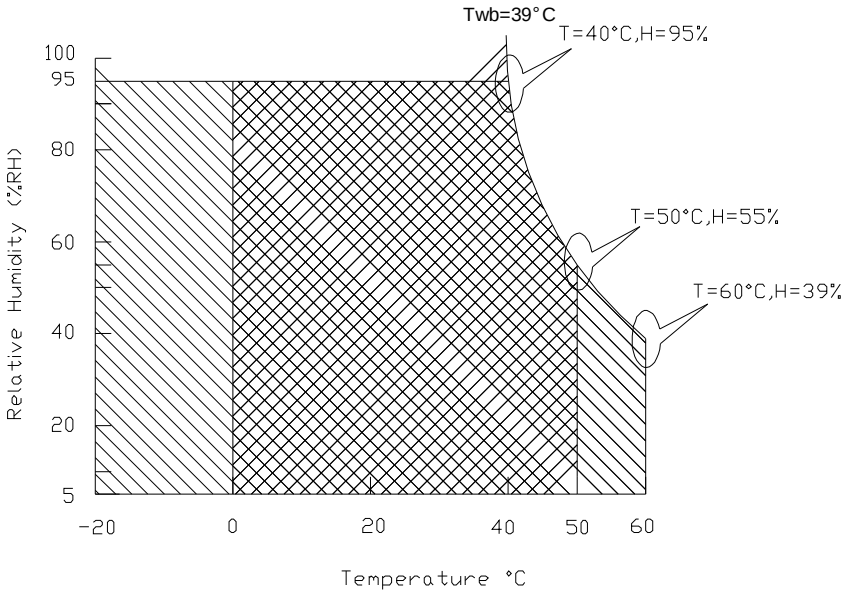
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: With in Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality perfermance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

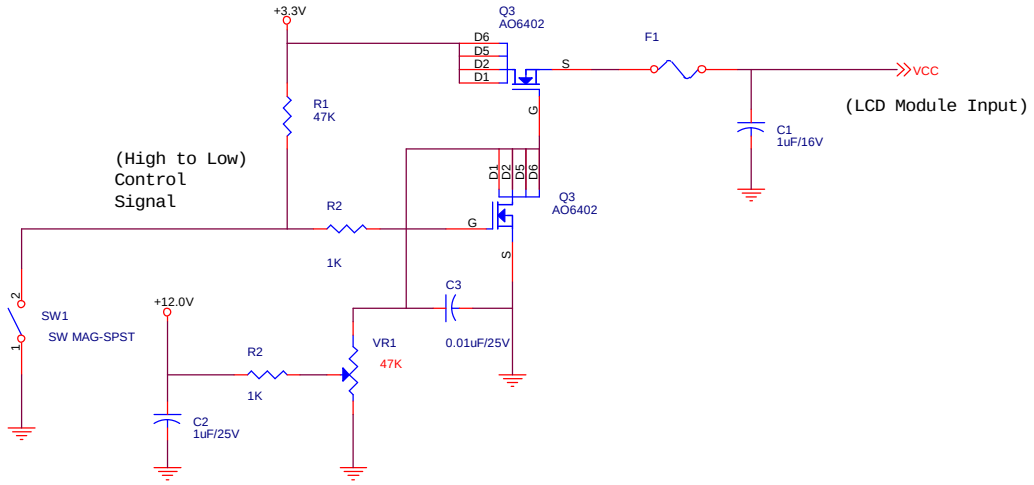
5.1 TFT LCD Module

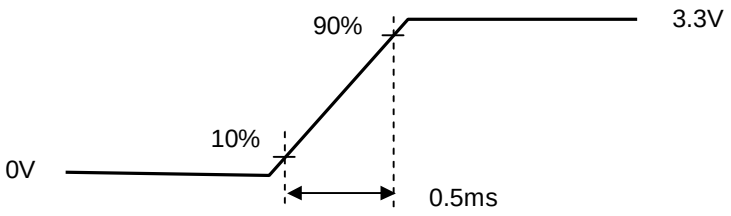
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		2.15		[Watt	All White pattern
IDD	IDD Current		680		mA	Max:All Black Pattern
IRush	Inrush Current			2000	mA	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

Note 1 : Measurement conditions:





Vin rising

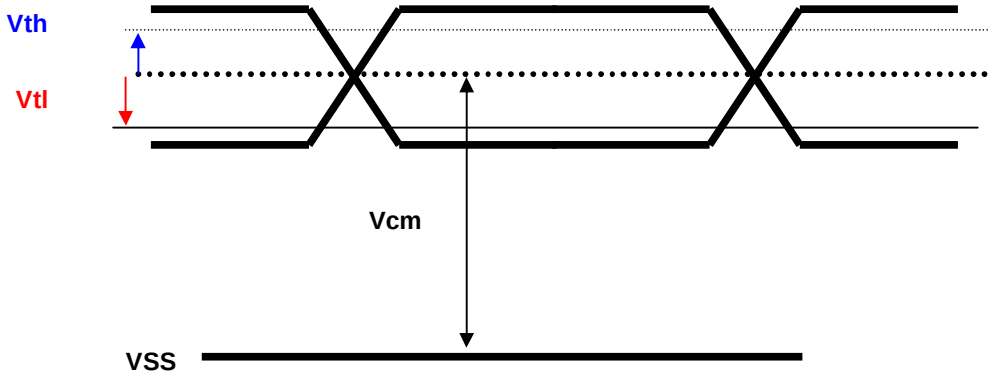
5.1.2 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A(Thine Electronics Inc.) in detail.Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	170	200	-	[cd/m^2]	(Ta=25℃)
CCFL current(ICCFL)	3.0	6.5	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCCFL)	45	50	80	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1500			[Volt] rms	(Ta= 0℃) Note 5
CCFL Voltage (Reference) (VCCFL)	745	785	905	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (PCCFL)		4.9		[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.

Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

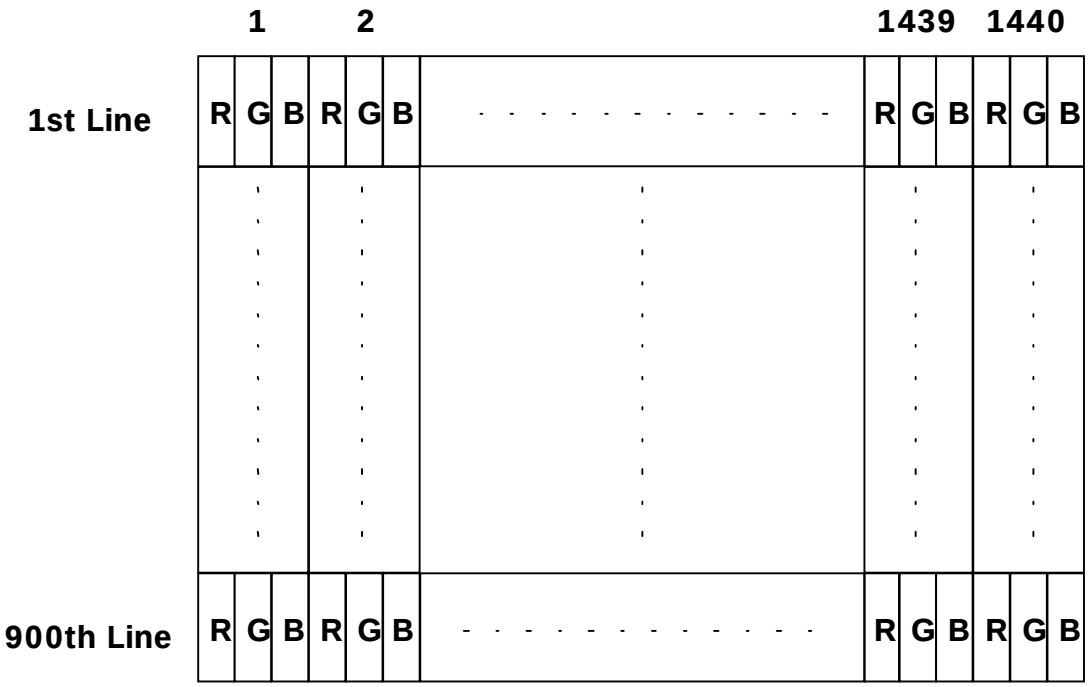
Note 5: CFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 6: Calculator value for reference (ICCFL×VCCFL=PCCFL)

6. Signal Characteristic

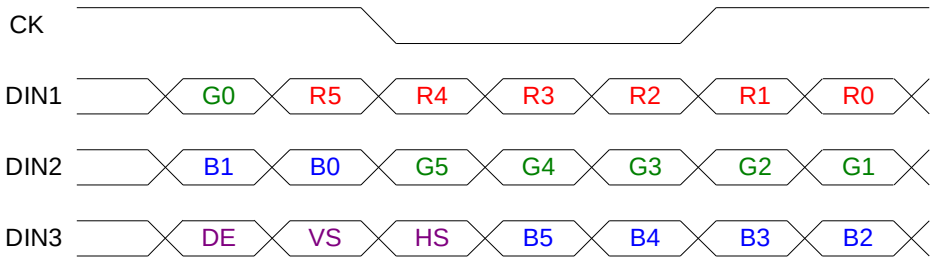
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

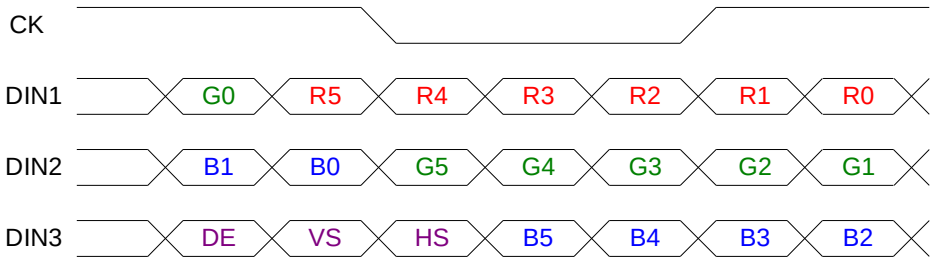


6.2 The input data format

ODD pair(1st pixel input)



Even pair(2nd pixel input)



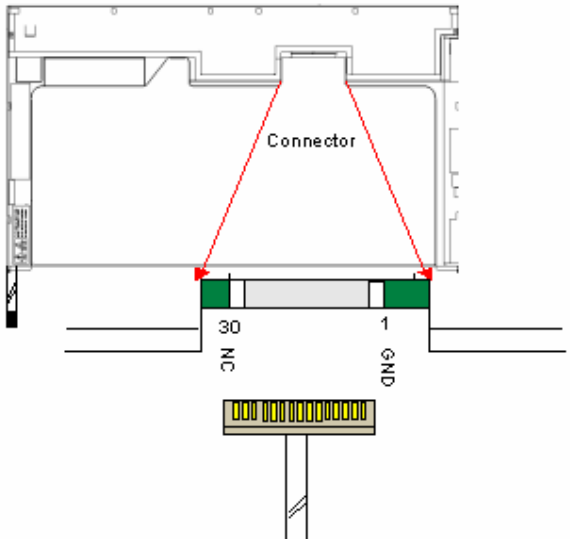
Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	**Data Clock**	The typical frequency is 48.2 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DE	**Display Timing**	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VS	**Vertical Sync**	The signal is synchronized to -DTCLK .
HS	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.3 Signal Description

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin no	Symbol	Function	Etc.
1	GND	Ground	
2	VDD	Power supply ,3.3 V (typical)	
3	VDD	Power supply ,3.3 V (typical)	
4	V_{EDID}	DDC 3.3V power	
5	NC	No Connection (Reserved for AUO) test	
6	CLK_{EDID}	DDC Clock	
7	$Data_{EDID}$	DDC data	
8	Odd_RxIN0-	-LVDS differential data input	
9	Odd_RxIN0+	+LVDS differential data input	
10	GND	Ground	
11	Odd_RxIN1-	-LVDS differential data input	
12	Odd_RxIN1+	+LVDS differential data input	
13	GND	Ground	
14	Odd_RxIN2-	-LVDS differential data input	
15	Odd_RxIN2+	+LVDS differential data input	
16	GND	Ground	
17	Odd_RxCLKIN-	-LVDS differential clock input	
18	Odd_RxCLKIN+	+LVDS differential clock input	
19	GND	Ground	
20	Even_RxIN0-	-LVDS differential data input	
21	Even_RxIN0+	+LVDS differential data input	
22	GND	Ground	
23	Even_RxIN1-	-LVDS differential data input	
24	Even_RxIN1+	+LVDS differential data input	
25	GND	Ground	
26	Even_RxIN2-	-LVDS differential data input	
27	Even_RxIN2+	+LVDS differential data input	
28	GND	Ground	
29	Even_RxCLKIN-	-LVDS differential clock input	
30	Even_RxCLKIN+	+LVDS differential clock input	

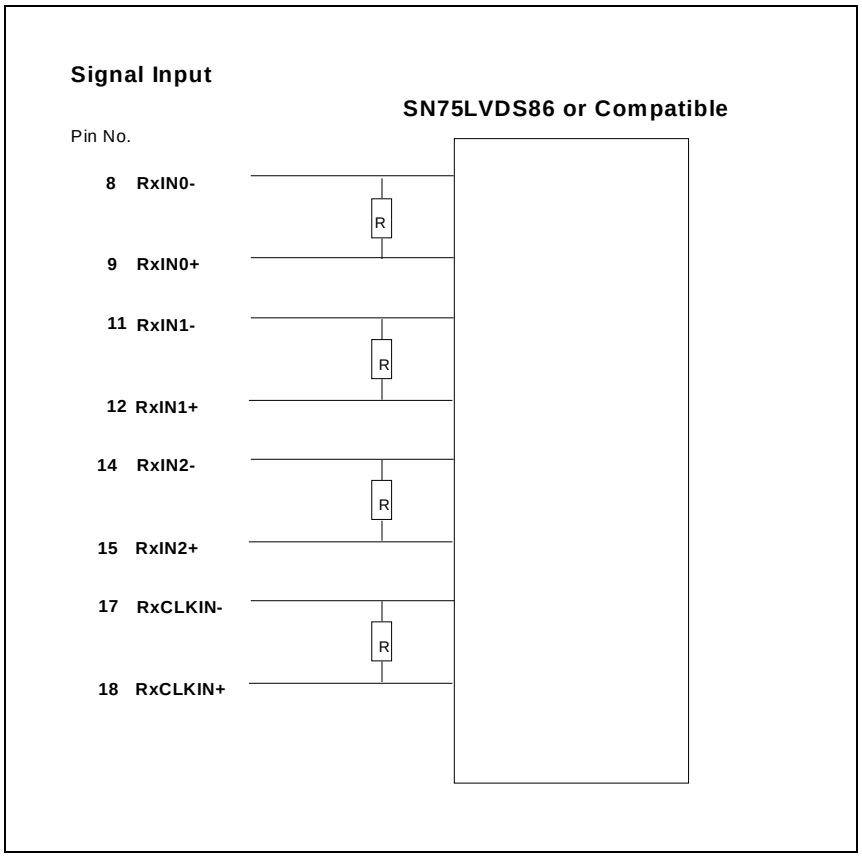


Note1: Start from right side

Note2: Please follow VESA standard.

Note3: Input signals shall be low or High-impedance when VDD is off.
Internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

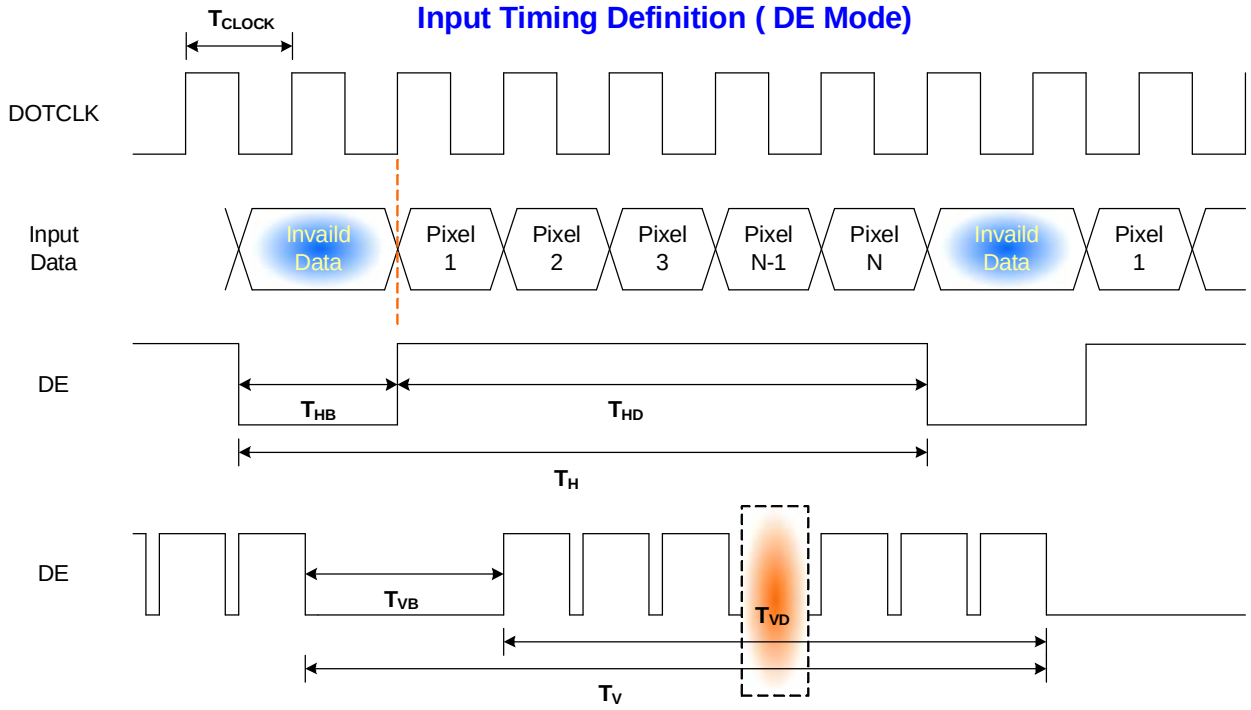
6.4.1 Timing Characteristics

Basically, interface timings should match the 1440x900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency		1/ T_{CLOCK}	20	48.2	85	MHz	LVDS 2 channel input
Horizontal Section	**Period**	T_H	840	880	1024	T_{CLOCK}	
	Active	T_{HD}	720	720	720		
	Blanking	T_{HB}	140	160	304		
	Hsync Width	T_{HSW}	10	16	20		
	Back Porch	T_{HSB}	98	112	142		
	Front Porch	T_{HSF}	142	32	142		
Vertical Section	**Period**	T_V	911	912	2048	T_{HD}	
	Active	T_{VD}	900	900	900		
	Blanking	T_{VB}	11	12	1148		
	Vsync Width	T_{VSW}	2	3	5		
	Back Porch	T_{VSB}	6	6	1140		
	Front Porch	T_{VSF}	3	3	3		

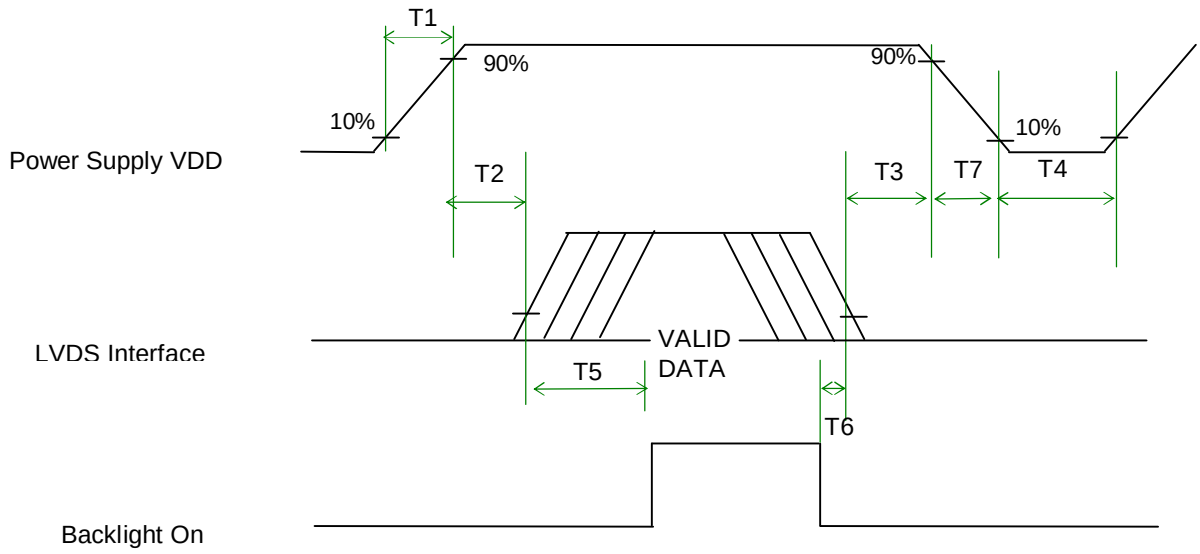
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H
Mating Contact/Part Number	FI-XC3-1-15000

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 180 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40℃/95%,300Hr	
High Temperature Operation	60℃/Dry,300Hr	
Low Temperature Operation	0℃,300Hr	
On/Off Test	25℃,150hrs(ON/10 sec. OFF/10sec., 10,000 cycles)	
Hot Storage	60℃/35% RH ,250 hours	
Cold Storage	-20℃/50% RH ,250 hours	
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles	
Hot Start Test	50℃/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0℃/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	180G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 1.5 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25℃, 2000hours, Operating with loop pattern	

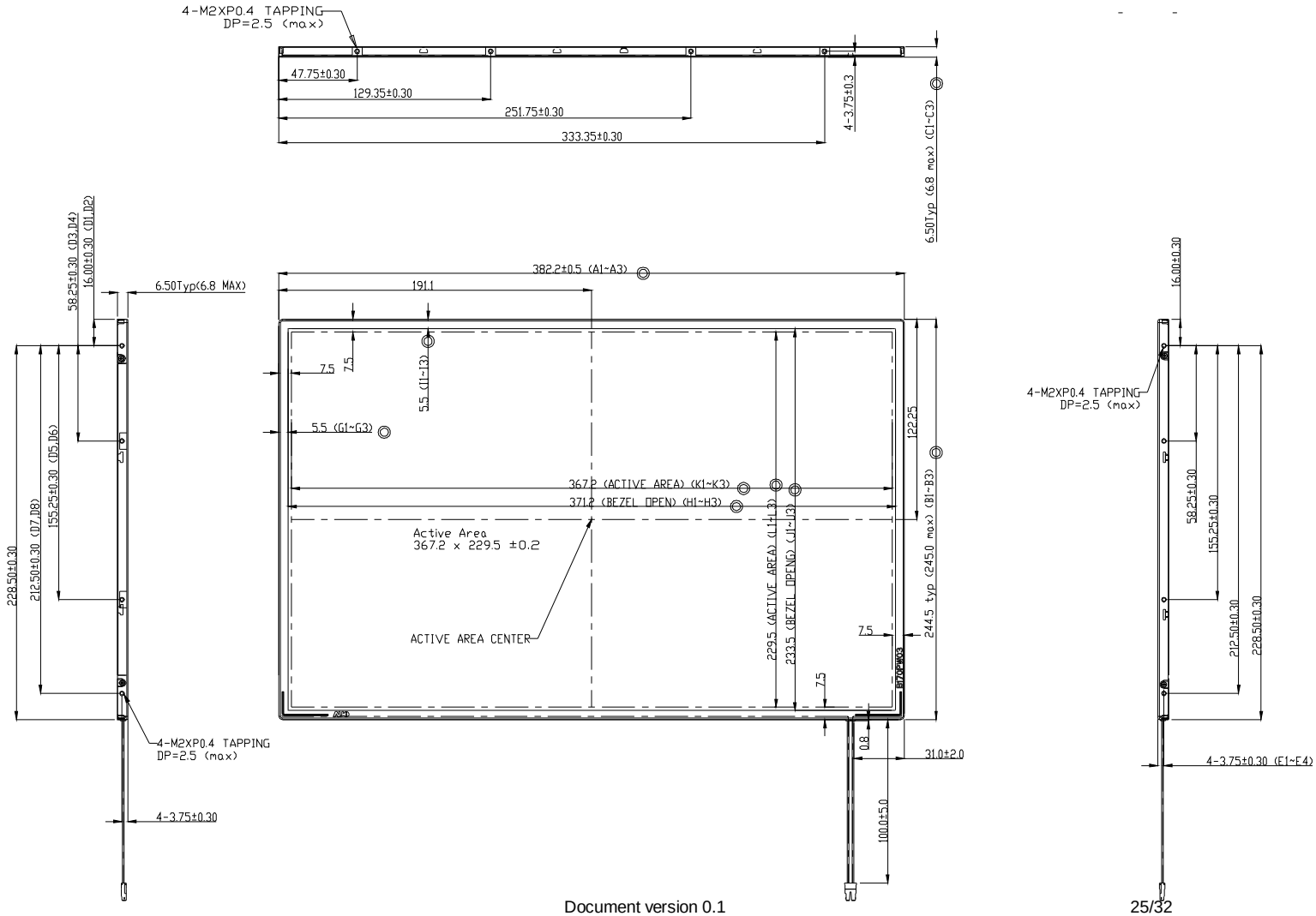
Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

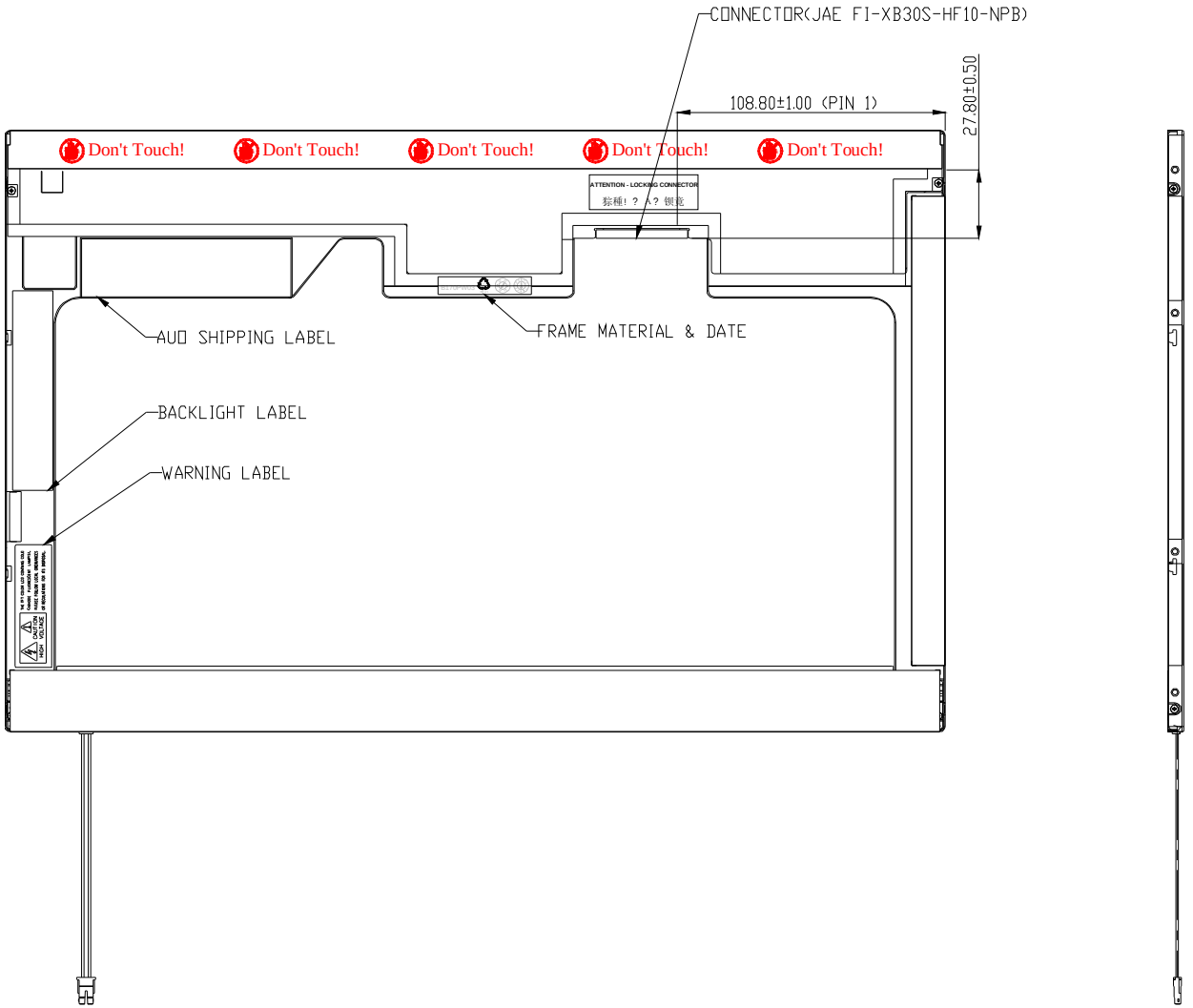
Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension(Front View)



10.2 LCM Outline Dimension(Rear View)



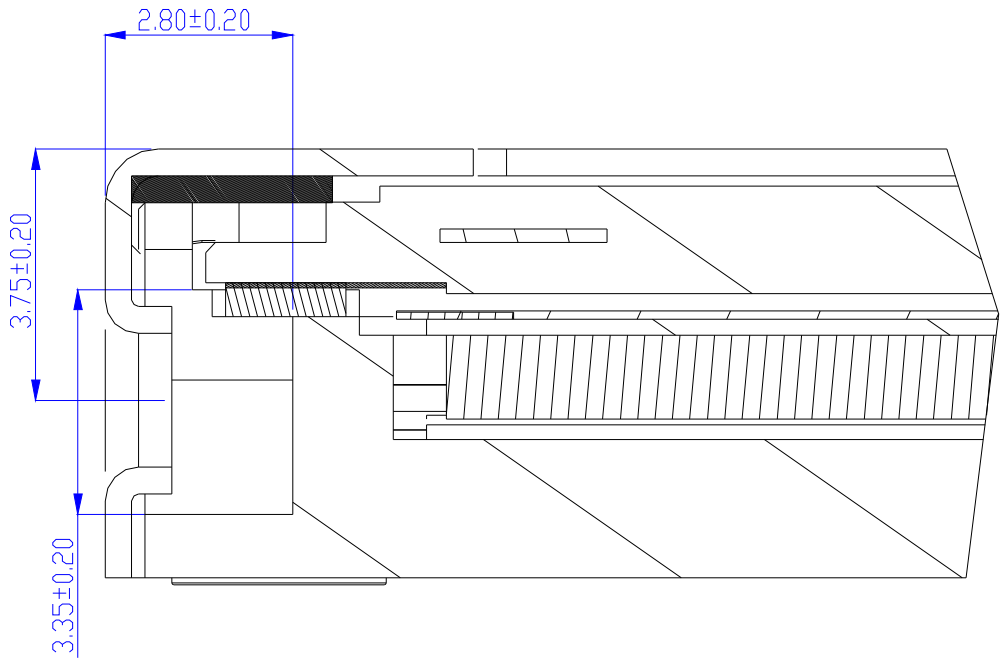
10.3 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.6 mm (See drawing)

Screw hole center location, from front surface = 3.75 ± 0.2mm (See drawing)

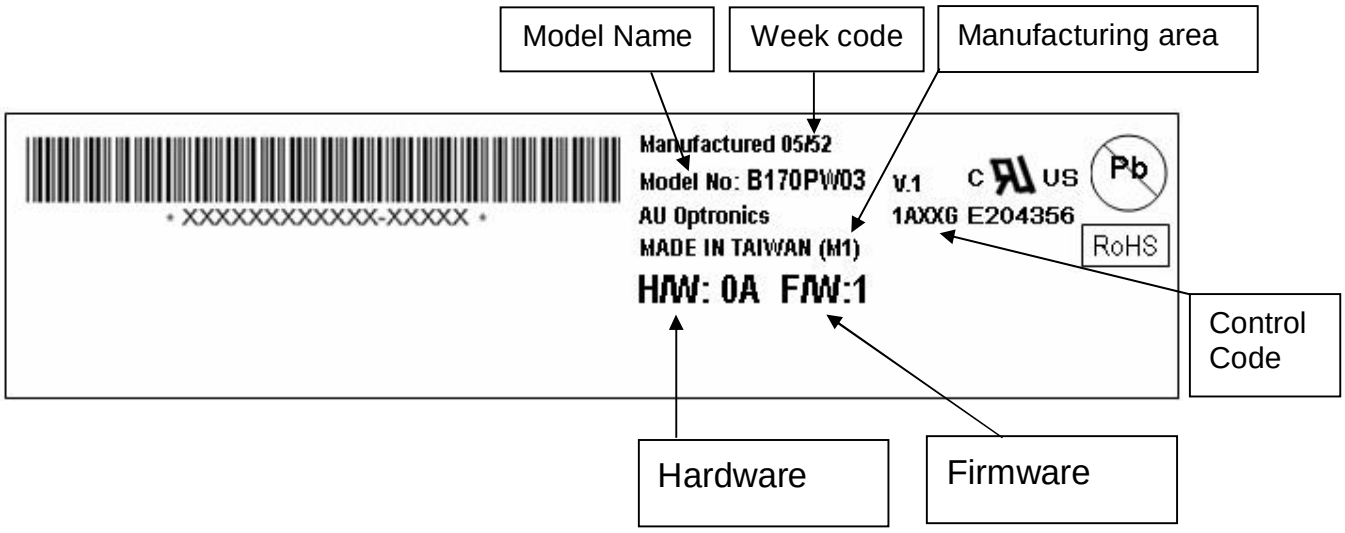
Screw maximum length = 2.3 mm (See drawing)

Screw Torque: Maximum2.5 kgzf-cm

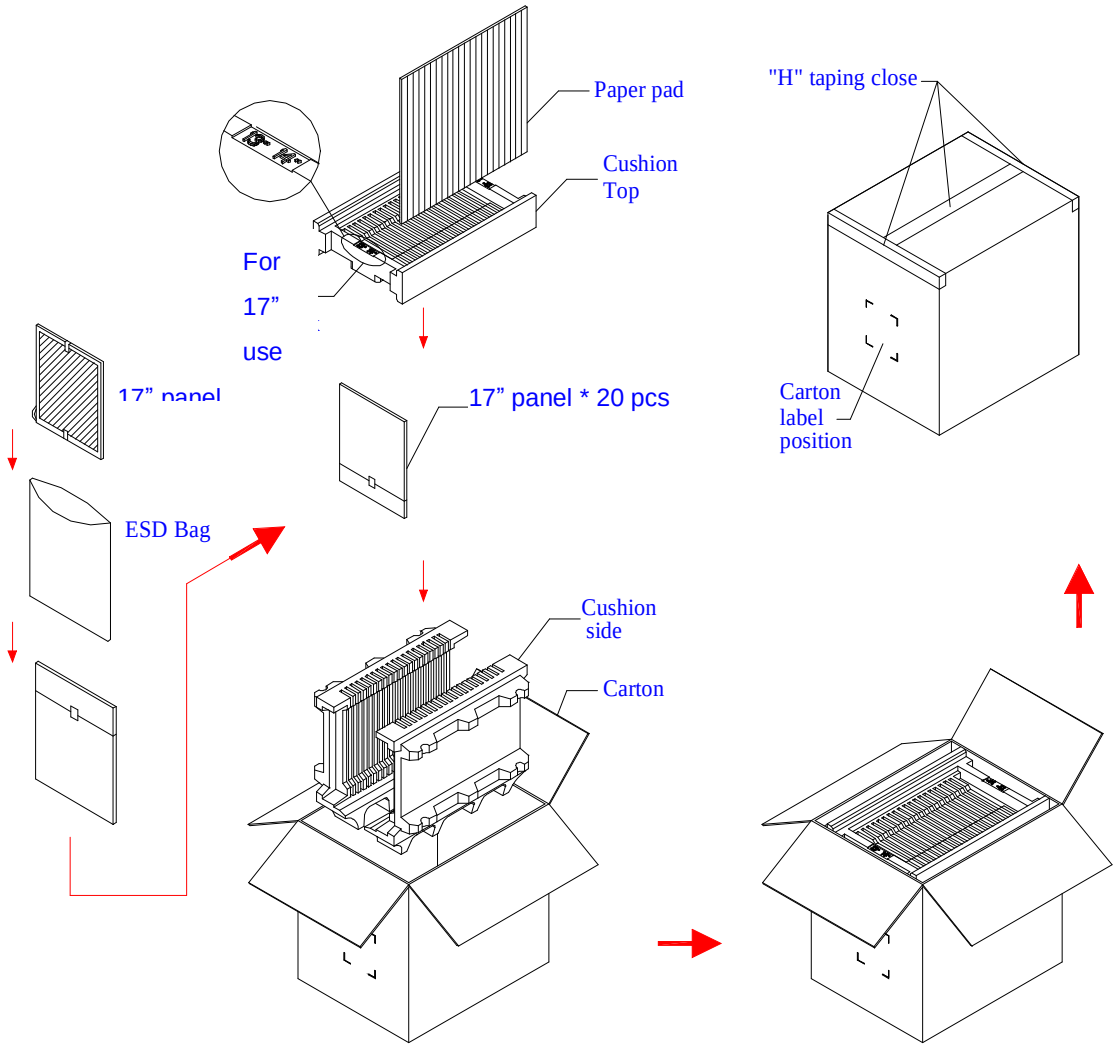


11. Shipping and Package

11.1 Shipping Label Format



11.2. Carton package



12. Appendix: EDID description

DEC	HEX	FUNCTION	HEX	BIN	DEC
			16 進位	2 進位	10 進位
0	0	EDID Header	00	00000000	0
1	1		FF	11111111	255
2	2		FF	11111111	255
3	3		FF	11111111	255
4	4		FF	11111111	255
5	5		FF	11111111	255
6	6		FF	11111111	255
7	7		00	00000000	0
8	8	EISA Manufacturer Code = 3 char ID	06	00000110	6
9	9		AF	10101111	175
10	0A	Product Code LSB = vendor code	87	10000111	135
11	0B	Product Code USB =	31	00110001	49
12	0C	ID(32-bit) serial Number	00	00000000	0
13	0D		00	00000000	0
14	0E		00	00000000	0
15	0F		00	00000000	0
16	10	Week of manufacture	01	00000001	1
17	11	Year of manufacture	0F	00001111	15
18	12	EDID Structure Ver. = 1	01	00000001	1
19	13	EDID revision = 3	03	00000011	3
20	14	Video input def. *(digital I/P, non-TMDS, CRGB)*	80	10000000	128
21	15	Max H image size *(rounded to cm)*	25	00100101	37
22	16	Max V image size *(rounded to cm)*	17	00010111	23
23	17	Display Gamma *(=(gamma*100)-100)*	78	01111000	120
24	18	Feature support *(no DPMS, Active OFF, RGB, tmg Blk#1)*	0A	00001010	10
25	19	Red/green low bits (Lower 2:2:2:2 bits)	6D	01101101	109
26	1A	Blue/white low bits (Lower 2:2:2:2 bits)	F2	11110010	242
27	1B	Red x (Upper 8 bits)	9C	10011100	156
28	1C	Red y	59	01011001	89
29	1D	Green x	4C	01001100	76
30	1E	Green y	8F	10001111	143
31	1F	Blue x	23	00100011	35
32	20	Blue y	23	00100011	35
33	21	White x	52	01010010	82
34	22	White y	54	01010100	84
35	23	Established timing 1	00	00000000	0
36	24	Established timing 2	00	00000000	0
37	25	Manufacturer's timings	00	00000000	0
38	26	Standard timing #1	01	00000001	1
39	27		01	00000001	1
40	28	Standard timing #2	01	00000001	1
41	29		01	00000001	1
42	2A	Standard timing #3	01	00000001	1
43	2B		01	00000001	1
44	2C	Standard timing #4	01	00000001	1
45	2D		01	00000001	1
46	2E	Standard timing #5	01	00000001	1
47	2F		01	00000001	1
48	30	Standard timing #6	01	00000001	1
49	31		01	00000001	1
50	32	Standard timing #7	01	00000001	1

51	33		01	00000001	1
52	34	Standard timing #8	01	00000001	1
53	35		01	00000001	1
54	36	Pixel Clock/10000 LSB	9E	10011110	158
55	37	Pixel Clock/10000 USB	25	00100101	37
56	38	Horz active Lower 8bits	A0	10100000	160
57	39	Horz blanking(Thbp) Lower 8bits	40	01000000	64
58	3A	HorzAct:HorzBlnk(Thbp) Upper 4:4 bits	51	01010001	81
59	3B	Vertical Active Lower 8bits	84	10000100	132
60	3C	Vertical Blanking(Tvbp) Lower 8bits	0C	00001100	12
61	3D	Vert Act : Vertical Blanking(Tvbp) (upper 4:4 bit)	30	00110000	48
62	3E	HorzSync. Offset (Thfp)	40	01000000	64
63	3F	HorzSync.Width	20	00100000	32
64	40	VertSync.Offset(Tvfp) : VertSync.Width	33	00110011	51
65	41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
66	42	Horizontal Image Size Lower 8bits	6F	01101111	111
67	43	Vertical Image Size Lower 8bits	E6	11100110	230
68	44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16
69	45	Horizontal Border *(zero for internal LCD)*	00	00000000	0
70	46	Vertical Border *(zero for internal LCD)*	00	00000000	0
71	47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24
72	48	Flag	00	00000000	0
73	49	Flag	00	00000000	0
74	4A	Flag	00	00000000	0
75	4B	ASCII Data String Tag: Manf defined: P/N	0F	00001111	15
76	4C	Flag	00	00000000	0
77	4D		00	00000000	0
78	4E		00	00000000	0
79	4F		00	00000000	0
80	50		00	00000000	0
81	51		00	00000000	0
82	52		00	00000000	0
83	53		00	00000000	0
84	54		00	00000000	0
85	55		00	00000000	0
86	56		00	00000000	0
87	57		00	00000000	0
88	58		00	00000000	0
89	59		20	00100000	32
90	5A	Flag	00	00000000	0
91	5B	Flag	00	00000000	0
92	5C	Flag	00	00000000	0
93	5D	ASCII Data String Tag: Manf defined: SUPPLIER	FE	11111110	254
94	5E	Flag	00	00000000	0
95	5F		41	01000001	65
96	60		55	01010101	85
97	61		4F	01001111	79
98	62		0A	00001010	10
99	63		20	00100000	32
100	64		20	00100000	32
101	65		20	00100000	32
102	66		20	00100000	32
103	67		20	00100000	32
104	68		20	00100000	32
105	69		20	00100000	32
106	6A		20	00100000	32
107	6B		20	00100000	32

108	6C	Flag	00	00000000	0
109	6D	Flag	00	00000000	0
110	6E	Flag	00	00000000	0
111	6F	ASCII Data String Tag: Manf defined: P/N	FE	11111110	254
112	70	Flag	00	00000000	0
113	71		42	01000010	66
114	72		31	00110001	49
115	73		37	00110111	55
116	74		30	00110000	48
117	75		50	01010000	80
118	76		57	01010111	87
119	77		30	00110000	48
120	78		33	00110011	51
121	79		20	00100000	32
122	7A		56	01010110	86
123	7B		31	00110001	49
124	7C		20	00100000	32
125	7D		0A	00001010	10
126	7E	Extension Flag	0	00000000	0
127	7F	Checksum	69		105